

BEST AVAILABLE COPY**LISTING OF THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the present application.

Claim 1 (Original) A method of forming an ultra thin fully-depleted silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) structure comprising the steps of:

providing a SOI structure comprising a dummy gate that has an upper surface that is coplanar with an upper surface of a planarizing material, said dummy gate is located on a sacrificial oxide that is positioned atop a top Si-containing layer of a SOI substrate;

removing the dummy gate to provide a gate opening that exposes a portion of the underlying sacrificial oxide layer, said gate opening defining a device channel in said top Si-containing layer;

implanting ions into the device channel, said ions comprise nitrogen or fluorine;

removing the sacrificial oxide layer to expose the device channel;

recessing the device channel to provide a recessed device channel; and

forming the gate, including gate dielectric and gate electrode in said opening atop the recessed device channel.

Claim 2 (Currently Amended) The method of Claim 1 wherein the providing the SOI structure ~~comprising~~ comprises forming said sacrificial oxide on a surface of said top Si-containing layer; forming a layer of dummy gate material; and patterning said layer of dummy gate material.

Claim 3 (Original) The method of Claim 1 wherein the removing the dummy gate comprises an etching process.

Claim 4 (Original) The method of Claim 3 wherein said etching process comprises chemical downstream etching or KOH etching.

Claim 5 (Original) The method of Claim 1 further comprising forming an outer insulating spacer on the dummy gate prior to forming said planarizing material.

Claim 6 (Original) The method of Claim 1 wherein said implanting said ions is performed at an ion dose from about $1E13$ to about $5E14$ atoms/cm².

Claim 7 (Original) The method of Claim 1 wherein said removing the sacrificial oxide comprises a chemical oxide removal (COR) step.

Claim 8 (Original) The method of Claim 7 wherein said COR step comprises a vapor or plasma of HF and NH₃.

Claim 9 (Original) The method of Claim 7 wherein said COR is performed at a pressure of about 6 millitorr or less.

Claim 10 (Original) The method of Claim 1 wherein said recessing the device channel comprises successive oxidation and COR etching steps.

Claim 11 (Original) The method of Claim 10 wherein said COR etching comprises a vapor or plasma of HF and NH_3 , said etching is performed at a pressure of about 6 millitorr or less.

Claim 12 (Original) The method of Claim 1 further comprising etching back said planarizing material.

Claim 13 (Original) The method of Claim 12 further comprising forming source/drain diffusion regions in said top Si-containing substrate after said etching back step.

Claims 14-18 (Cancelled)